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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/945,394	KIRK, STEVE VAN	
	Examiner	Art Unit	
	Tuan T Dinh	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-65* is/are pending in the application.

4a) Of the above claim(s) *5-19,21-27,31-33,39-43 and 49-64* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,20,28-30,34-38,44-48 and 65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election with traverse of Group I (claims 1-6, 8-11, 19-22, 24-40, and 42-48) in Paper No. 7 is acknowledged.

The traversal is on the ground(s) that claim 50 is read on a process used in the restriction requirement.

This is not found persuasive because claim 50 recited "the method of forming a circuit board having first and second conductive layers comprising: forming first and second interstices in the first and second conductive layers, inserting a dielectric layer between the first and second interstices, then engaging the first and second interstice" which is different process in the restriction being used, the restriction requirement states that: "forming a dielectric layer (first), forming first and second conductive layers having first and second interstices on top and bottom surfaces of the dielectric layer (second), then engaging the interstices" which is mean by "forming a dielectric layer first and forming conductive layers on top and bottom surfaces of the dielectric layer" in stead of "forming conductive layers first then inserting a dielectric layer interposed therebetween".

The requirement is still deemed proper and is therefore made FINAL. Claims 5-6, 10-11 having the limitations "horizontally-opposited and vertically overlapping" would read on figure 11, claims 8-9 having the limitations "a first conductive layer sinuously interwined" would read on figures 4, 7-8, claim 19 having "...the second interstice has a plurality of second widths laying in a second plane" would read on figures 12-13, claims

21-22, and 26-27 would read on figures 9-11, claims 31-33 would read on figure 11, claims 39-40 would read on figure 11. Since applicant in paper #5 did not elect figures 4, and 7-11 because species of restriction requirement. Therefore, claims 5-6, 8-11, 19, 21-27, 31-33, and 39-40, 42-43 are withdrawn from further consideration as being drawn to non-elected subject matter. New claim 65 is now join to group I.

The remaining claims now are 1-4, 20, 28-30, 34-38, and 65 that would be exam as shown below:

Drawings

2. The drawings are objected to because:

the "cross-hatching of first and second conducive layers, a dielectric layer is improper" and a capacitor having a dielectric layer, claims 28, 34, line 4" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Examiner suggest applicant to see MPEP 608.02, page 600-84 for cross-hatching purpose.

The drawings are objected to because there are two duplicate pages 8 and 9 show the same figures 13 and 14.

Figure 15 is object because a second conductive layer does not show to include a second interstice. However, the figure 15 shows the second conductive layer, which seems to be a single planar conductive layer, and not include the second interstice.

The drawings are objected to under 37 CFR 1.83(a) because they fail to show "the first and second interstices 150, 160" in figure 15 as described in the specification.

Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d).

Also, applicant should clarify in what intended of "the broken line" means to in the figure 15.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 20 and 43 are objected to because of the following informalities:

Claim 20, line 5, "the second" should be change to –the second interstice—for proper antecedent basis.

Claim 20, line 8, "the first plurality of widths" should be change to—the plurality of first widths—for proper antecedent basis.

Applicant recites claims 43, which is depending on claim 40, since claim 40 is withdrawn from further consideration as being drawn to non-elected claim as explained as above (portion 1). Examiner suggests amending or canceling claim 43 for proper depending claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 2-4, 28-30, and 34-37 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claims 2-4, the specification does not proper describe "first and second conductive layer are power and ground planes of the circuit board" applicant should clarify these limitations in the specification, and further, the drawings do not show the first and second conductive layers, which are power and ground planes.

Regarding claims 28 and 34, the specification does not proper describe "a capacitor having a dielectric layer...second interstice" Applicant should clarify this limitation in the specification and drawings. It is understood by examiner to assume that "a capacitor...second interstice" should be --a dielectric layer having a capacitance...second interstice--.

Regarding claim 45, the specification does not proper describe "a circuit board having a power plane...ground plane..." Applicant should clarify and define these limitations in specification and drawing.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-4, 20, 28-30, 34-38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, it is confuse. The phrase of "...including a second interstice engaged with the first interstice, and a dielectric layer disposed between the first and second interstices" is not understood. Does applicant mean of " the second interstice engaged with the first interstice by a dielectric layer disposed therebetween?"

Examiner suggest that claim 1, lines 3-5 should be -- ...including a second interstice engaged with the first interstice by a dielectric layer disposed therebetween— for proper reading.

Regarding claim 20, it is unclear. Same as explained in claim 1, examiner suggests to change in lines 4 and 6 should be –...a second interstice engaged by a dielectric layer with the first interstice —, and delete "a dielectric layer disposed between the first and second interstices" for proper reading.

Regarding claim 20, it is confuse, Does applicant mean of "a first interstice has a plurality of first width, which are the same or different widths? Also, applicant should clarify the limitation of "a second conductive layer including a second interstice, and the second interstice has a single second width" because there is no support in the specification and the drawings (specific in figure 15).

Regarding claim 28, it is unclear. Same as explained of claim 1, examiner suggest to change in lines 4-5 should be –a dielectric layer having a capacitance disposed between and engaged the first and second interstices—for proper reading.

Regarding claim 34, it is unclear. Same as explained of claim 1, examiner suggest to change in lines 4-5 should be –a dielectric layer having a capacitance disposed between and engaged the first and second interstices—for proper reading.

Regarding claim 36, it is unclear. The phrase of "the dielectric layer...provided a pre-selected amount of capacitance between the first and second conductive layers" is not understood. Applicant should clarify what is intended by "pre-selected amount of capacitance" since the dielectric layer made by a dielectric material having a dielectric constant. The dielectric constant can be high or low depends on what applicable being used, for example, with high dielectric constant performing a bypass capacitance function, and with a low dielectric constant performing a minimize the high frequency losses. The ideal of chosen the dielectric layer having its dielectric constant to perform a bypass capacitance or minimize the high frequency losses already set to apply in a multiplayer circuit board. How applicant can "pre-selected amount of capacitance" of the dielectric constant of the dielectric layer?

Regarding claim 37, it is unclear. The phrase of "a degree of overlap...for the capacitor" doe not appear in the specification and drawings, and also, what does applicant mean of "pre-selected amount of capacitance" applicant should clarify what is intended by "pre-selected amount of capacitance"

Regarding claim 38, it is unclear. Same as explained of claim 1, examiner suggest to change in lines 5-6 should be –...second interstice engaged with the first interstice by a dielectric layer disposed therebetween—for proper reading.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-4, 28, 38, and 65, are rejected under 35 U.S.C. 102(b) as being anticipated by Nakao et al. (U. S. Patent 5,926,377).

As best understood to claims 1-4 28, 38, and 65, Nakao et al. discloses a circuit board as shown in figures 2 and 16a-16b comprising:

a first conductive layer (23) including a first interstice (50), which is a power plane;

a second conductive layer (25) including a second interstice (51), which is a ground plane, and engaged with the first interstice by a dielectric layer (24) having a capacitance (impedance) disposed between the first and second interstices (50, 51).

As best understood to claim 20, Nakao et al. discloses a circuit board as shown in figures 16a-16b comprising:

a first conductive layer (23) including a first interstice, wherein the first interstice has a first width laying in a first plane;

a second conductive layer (25) including a second interstice engaged with the first interstice by a dielectric layer disposed between the first and second interstices, wherein the second has a second width laying in a second plane; and

wherein the first and second planes are substantially parallel.

As to claim 38, Nakao et al. discloses an electronic circuit as shown in figures 1-16 comprising:

a first power terminal (100, see an attached paper sketching in figure 6b to show a first power terminal) operationally connected to a first conductive layer (23) having a first interstice (50);

a second power terminal (200, see an attached paper sketching in figure 6b to show a second power terminal) operationally connected to a second conductive layer (25) having a second interstice (51) engaged with the first interstice by a dielectric layer (24) disposed therebetween.

As to claim 65, Nakao et al. discloses a circuit board having first and second conductive layers (23, 25) as shown in figures 1-16 comprising:

means for forming a first interstice (50) in the first conductive layer;

means for forming a second interstice (51) in the second conductive layer;

means for inserting a dielectric layer (24) between the first and second interstices; and

means for engaging the first and second interstices by the dielectric layer (24).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakao et al. ('377) in view of Novak (U. S. Patent 6,215,372).

Regarding claims 28-29, Nakao et al. does not disclose the dielectric layer having a dielectric constant about 3 to 5.

Novak shows the dielectric layer (412) formed between power and ground layers (414, 412) having a dielectric constant about 4.7 (column 2, lines 47-48).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a dielectric layer having a dielectric constant about 3-5 in the circuit board of Nakao et al., as taught by Novak et al., for the purpose of reducing a power supply impedance and increasing charge storage in the dielectric layer.

12. Claims 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakao et al. ('377) in view of Lee et al. (U. S. Patent 5,497,037).

As to claims 34-37, Nakao et al. discloses a circuit board as shown in figures 1-16 having first and second conductive layers (23, 25), wherein the first conductive layer (23) includes a first interstice (50) and the second conductive layer (25) includes a second interstice (51), the circuit board comprising:

a dielectric layer (24) having a capacitance disposed between and engaged the first and second interstices (50, 51); and an electrical circuit (see figure 16a shown components mounted on the circuit board) mounted to the circuit board.

It is noted that Nakao et al does not specifically disclose the first and second conductive layers are connected to first and second power supply voltages respectively, and the electrical circuit are powered by the first and second power supply voltages. However, it is well know in the art of high speed signal processing that the power supply voltage must be present in the circuit board to provide DC/AC power to operate components in the circuit board. Therefore, Nakao et al. does not need to specifically show the power supply voltage in the disclosure since one skill in the art is presumed to know something about the art apart from what the references literally disclose. Note In re Jacoby, 309 F.2d 513, 135 USPQ 317 (CCPA 1962). It is also well settled that obviousness may be concluded from common knowledge and common sense of the person skilled in the art without a specific hint or suggestion. In re Bozek, 416 F.2d 1385, 163 USPQ 545 (CCPA 1969). Nevertheless, for the applicant benefic, the examiner submits an additional reference, Lee et al, which discloses power supply voltages (105) having 3.3V connected to first and second conductive layers (103, 104), see figure 4 for the purpose of providing DC and AC voltages.

As to claim 44, Nakao et al. discloses a power supply system in figures 6a-6b-16a-16b, comprising:

first power and ground terminals (100, 200);

first and second conductive layers (23, 25) having first and second interstice and engaged by a dielectric layer disposed between, as explained in claim 1.

Nakao et al does not disclose having first and second power supplies. However, Lee et al shows a printed circuit board (PCB) in figures 2 and 4 comprising first and second power supplies (16-figure 2) or (105-figure 4).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize two power supplies in the system of Nakao et al, as taught by Lee et al. in for the purpose of providing DC/DC or DC/AC voltage power.

13. Claims 45-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakao et al. ('377) in view of Takeshita et al. (US 6,469,259).

Regarding claims 45-46, Nakao et al. discloses all of the limitation as explained in claims 1-4, except for component, which is connected to the first and second conductive layers (or power and ground planes), is a memory chip or processor.

Takeshita et al. shows a wiring board comprising a semiconductor device (4), which is an IC or LSI connected to power and ground layers (5,6), see column 5, lines 10-19.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ a memory chip or a processor in the memory circuit module or a computer system of Nakao et al, as taught by Takeshita et al., for the purpose of providing high frequency current.

As to claims 47-48, Nakao et al discloses the first and second interstices are formed in complementary or complementary rectangular shapes.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Iguchi et al., Harada et al., and Novak disclose related art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Dinh
March 05, 2004.

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800